17

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/046,671 | 03/24/1998 | MASATO TAKITA | P8077-8003 | 2422 |

7590 10/16/2003

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 CONNECTICUT AVENUE NW SUITE 600
WASHINGTON, DC 20036-5339

| EXAMINER | |
|---|---|
| MALDONADO, JULIO J | |
| ART UNIT | PAPER NUMBER |
| 2823 | |

DATE MAILED: 10/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/046,671 | TAKITA ET AL. | |
| | Examiner | Art Unit | |
| | Julio J. Maldonado | 2823 | |

*-- Th MAILING DATE of this communication appears on the cover sheet with th correspondenc address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments, see remarks, filed 09/23/2003, with respect to the rejection(s)of claim(s) 1-7 under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Iwatani (U.S. 4,523,215).

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicants admitted prior art in the instant application in view of Iwatani (U.S. 4,523,215).

In reference to claim 1, the prior art (Instant Figs.29A-B) teaches a memory device including a lightly doped semiconductor substrate (114) of a first conduction type; a buried semiconductor layer of a second conduction type formed in a first region of the semiconductor substrate (114), spaced from a surface of the semiconductor substrate (114); a semiconductor region of the second conduction type (138) extending from the surface of the semiconductor substrate to a peripheral portion of the buried semiconductor layer, the semiconductor region of the second conduction type (138)

being connected to the buried semiconductor layer; and a semiconductor region of the first conduction type (164) formed in the semiconductor substrate (114) surrounded by the buried semiconductor layer and the semiconductor region (138) of the second conduction type, the semiconductor region of the first conduction type (164) being isolated from the semiconductor substrate (114) by the buried semiconductor layer and the semiconductor region of the second conduction type (138) (Instant page 4, line 13 – page 7, line 14).

The prior art fails to teach the semiconductor region of the first conductivity type has an equal concentration of impurity as that of the semiconductor substrate. However, Iwatani (Fig.1) in a related art to the formation of a PN junction isolation region teaches a semiconductor substrate (12, 16) of the first conductivity type; a buried semiconductor layer (14) of a second conduction type formed in a first region of the semiconductor substrate (12, 16), spaced from a surface of the semiconductor substrate (12, 16); a semiconductor region (20) of the second conductor type extending form the surface of the semiconductor substrate (12, 16) to a peripheral portion of the buried semiconductor layer (14), the semiconductor region (20) of the second conduction type being connected to the buried semiconductor layer (14); and a semiconductor region (22) of the first conduction type formed in the semiconductor substrate (12, 16) surrounded by the buried semiconductor layer (14) and the semiconductor region (20) of the second conduction type, the semiconductor region (22) of the first conduction type being isolated form the semiconductor substrate (12, 16) by the buried semiconductor layer (14) and the semiconductor region (20) of the

second conduction type, wherein a concentration of an impurity in the semiconductor region (22) of the first conduction type is equal to a concentration of an impurity in the semiconductor substrate (12, 16) (column 2, line 54 – column 3, line 59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the prior art and Iwatani to enable the region of the first conduction type to have the same concentration of impurities as that of the substrate as taught by Iwatani in the device of the prior art.

In reference to claim 2, the prior art further includes a first semiconductor element formed in the first conduction type region; and a second semiconductor element formed in a second region different from the first region of the semiconductor substrate, wherein the first conduction type semiconductor region is connected to a first potential, and wherein the second region of the semiconductor substrate is connected to a second potential different from the first potential (Instant Figs.28-29B and page 4, line 13 – page 7, line 14).

In reference to claim 3, the prior art shows wherein the second conduction type semiconductor region is extended over a third region adjacent to the first region of the semiconductor substrate; wherein the semiconductor device further includes a third semiconductor element formed in the third region of the second conduction type semiconductor region; and wherein the second conduction type semiconductor region is connected to a third potential different at least from the first potential or the second potential (Instant Figs.28-29B and page 4, line 13 – page 7, line 14).

In reference to claim 4, the prior art further includes a well of the first conduction type formed in a fourth region in the third region; and a fourth semiconductor element formed in the first conduction type well, wherein the first conduction type well is connected to a fourth potential different from at least the first potential (Instant Figs.28-29B and page 4, line 13 – page 7, line 14).

In re claims 5-7, the prior art further includes a first semiconductor element formed in the first conduction type region; and a second semiconductor element formed in a second region different from the first region of the semiconductor substrate, and that the second region of the semiconductor substrate is connected to a first potential, and wherein the second region of the semiconductor substrate is connected to a second potential different from the first potential. Applicants admitted prior art further teaches that the first semiconductor element and the second semiconductor element include a memory cell (Instant Figs.28-29B and page 4, line 13 – page 7, line 14).

***Response to Arguments***

4. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

5. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November

1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

JMR
10/3/03

George Fourson
Primary Examiner